

**Code No: C5705****JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****M.Tech I Semester Examinations March/April-2011****HARDWARE SOFTWARE CO-DESIGN****(VLSI SYSTEM DESIGN)****Time: 3hours****Max.Marks:60**

**Answer any five questions**  
**All questions carry equal marks**

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- 1.a) Draw and explain the Register Transfer level Block diagram of Design Model.  
b) With block diagram explain RISC with hardwired control. [12]
- 2.a) Briefly explain performance estimation.  
b) Explain different component specialization techniques. [12]
- 3.a) Explain about Aptix Prototyping System.  
b) Explain about Architecture of 8051 Micro Controller. [12]
- 4.a) Explain Commercial support of embedded processors.  
b) Are traditional Compilation techniques enough? Explain. [12]
- 5.a) Briefly explain about Compiler validation.  
b) Explain about The Co-design Computational model. [12]
- 6.a) Explain about Design verification.  
b) Compare Blocking Operations and Non-blocking Operations. [12]
- 7.a) Briefly explain about Synthesis Intermediate forms.  
b) Explain about Co-simulation Models. [12]
8. Write short notes on any **TWO** of the following:  
i) The Cosyma System  
ii) Interface Verification  
iii) System Communication infrastructure. [12]

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